AMENDMENT TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application and reflects amendments over the most recent version of the claims. A clean version of the claims is provided with the substitute specification filed herewith at Tab A.

Listing of Claims

1. (Currently Amended) An integrated read-only memory, comprising

having a plurality of selection transistors each having a drain connection,

having an electrode for feeding a voltage or a current;

having a layer between the each drain connections and the electrode, having a modifiable the electrical resistance of which can be changed through the effect of a configuration voltage or a configuration currentelectrical signal,

having a source connection per selection transistor;

having a bit line that is electrically connected to at least one source connection;

in which where the layer is formed as a common layer for linking the drain connections to the electrode, and

in which where the electrical resistance of the layer can be changed locally.

2. (Currently Amended) The read-only memory as claimed in of claim 1, in which where the resistance of the layer can be switched over.

3. (Currently Amended) The read-only memory as claimed in of claim 1 or 2, in which where the resistance of the layer can be switched over between two multiple resistance characteristic curves.

4. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claims 1, comprising:

~~having~~ a read ~~voltage~~ signal applied to the layer ~~or a read current fed to the layer~~ within a defined ~~voltage or current~~ signal range in a read operation of the read-only memory, and

~~having~~ a configuration ~~voltage or a configuration current~~ signal outside the ~~voltage or current~~ read signal range ~~provided for the read operation~~ in a configuration operation of the read-only memory.

5. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claim 1s, ~~which~~ where the read-only memoryis ~~designed as~~ a flash memory.

6. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claims 1, ~~in which~~ where the selection transistors are arranged in an array.

7. (Currently Amended) The read-only memory ~~as claimed in one~~ of claims ~~1 to 6~~, ~~in which~~ where the bit line is connected to a decoder circuit.

8. (Currently Amended) The read-only memory ~~as claimed in one~~ of claims 1 ~~to 7~~, ~~in which~~ where the bit line is accessible for an external connection.

9. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claims 1, comprising:

~~having~~ a gate connection per selection transistor~~;~~, and

~~having~~ a word line ~~that is~~ being electrically connected to at least one gate connection.

10. (Currently Amended) The read-only ~~memory as claimed in~~ of claim 9, ~~in which~~ where the word line is connected to a decoder circuit.

11. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 9 ~~or claim 10~~, ~~in which~~ where the word line is accessible for an external connection.

12. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claims 9, ~~in which~~ where the selection transistors have a substantially planar construction in the substrate.

13. (Currently Amended) The read-only memory ~~as claimed in one of~~ of claims ~~1 to 11~~, ~~in which~~ where the selection transistors have a vertical construction in the substrate.

14. (Currently Amended) The read-only memory ~~as claimed in one of the preceding~~ of claims 1, ~~in which~~ where the layer is formed as a molecular layer.

15. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains rotaxane.

16. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains catenane.

17. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ where the layer contains a bispyridinium compound.

18. (Currently Amended) The read-only memory ~~as claimed in one~~ of claims ~~1 to 13~~, ~~in which~~ where the layer is formed as a dielectric.

19. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 18, ~~in which~~ where the layer contains $SrZrO_3$.

20. (Currently Amended) The read-only memory ~~as claimed in one~~ of claims ~~1 to 13~~, ~~in which~~ where the layer is formed as a polymer.

21. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ where the layer contains 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

22. (Currently Amended) The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ where the layer contains a chalcogenide compound.

23. (Currently Amended) A method for operating an integrated read-only memory having a plurality of selection transistors each having a drain connection and an electrode for feeding a voltage or a current, including a layer between each drain connection and the electrode, ~~as claimed in one of the preceding claims~~, comprising:

providing a layer between each drain connection and the electrode, they layer having a modifiable electrical resistance through a configuration electrical signal, where the layer is formed as a common layer for linking the drain connections to the electrode, and where the electrical resistance of the layer can be changed locally;

applying ~~in which~~ in a read operation, a read voltage or a read current within a defined voltage or current range is applied to the layer~~,~~; and

applying ~~in which,~~ in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read operation is applied to the layer.

24. (Currently Amended) A method for producing an integrated read-only memory, comprising:

~~in which~~ producing an array of selection transistors ~~is produced~~ using CMOS technology~~,~~;

~~in which~~ leading drain contacts of the selection transistors ~~are led~~ to the surface of the arrangement~~,~~;

~~in which~~ depositing a layer ~~is deposited whose~~ having an electrical resistance that can be changed through the effect of a configuration ~~voltage or a configuration current~~signal, ~~it being possible for~~ where the electrical resistance of the layer ~~to~~ may be changed locally~~,~~;

~~in which~~ arranging an electrode is arranged above the layer~~,~~;

~~in which~~ forming a source connection ~~is formed~~ per selection transistor~~,~~;

~~in which~~ forming a bit line ~~is formed~~ which is electrically connected to at least one source connection~~,~~; and

~~in which~~ forming the layer ~~is formed~~ as a common layer for linking the drain connections to the electrode.

25. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 24, ~~in which~~ where the layer is deposited as a common layer for linking the drain connections to the electrode above the selection transistors.

26. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 24 ~~or claim 25~~, ~~in which~~ where the selection transistors are produced in a front end process.

27. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 26~~, ~~in which~~ where the layer is deposited in a back end process.

28. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 27~~, ~~in which~~ where the selection transistors are constructed in substantially planar fashion in the substrate.

29. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 27~~, ~~in which~~ where the selection transistors are constructed vertically in the substrate.

30. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ where the layer is formed as a molecular layer.

31. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains rotaxane.

32. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains catenane.

33. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ where the layer contains a bispyridinium compound.

34. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 29~~, ~~in which~~ where the layer is formed as a dielectric.

35. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in~~ of claim 34, ~~in which~~ where the layer contains $SrZrO_3$.

36. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 29~~, ~~in which~~ where the layer is formed as a polymer.

37. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed~~ of ~~in~~ claim 36, ~~in which~~ where the layer contains a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

38. (Currently Amended) The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 29~~, ~~in which~~ where the layer contains a chalcogenide compound.